REMARKS/ARGUMENTS

Claims 1-16, 18, 20, and 21 remain in the application.

I. SUMMARY OF THE APRIL 23RD, 2004 OFFICE ACTION

A. Rejection of Claims 1-6

Claims 1-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ziger U.S. Patent 6,498,640, and further in view of Stirton U.S. Patent 6,614,540.

B. Rejection of Claims 8-16

Claims 8-16 were rejected 35 U.S.C. § 103(a) as being unpatentable over Ziger U.S. Patent 6,498,640, and further in view of Stirton U.S. Patent 6,614,540.

C. Rejection of Claims 18, 20, and 21

Although page 1 of the Office Action mailed April 23, 2004 includes claims 18, 20, and 21 in the list of rejected claims, and pages 7-10 refer to the rejection of claims 18, 20, and 21, the Office Action recites no specific statutory grounds for the rejection of these three claims. That is, the Rejection does not specify whether the respective rejections of claims 18, 20, and 21 are under 35 U.S.C. § 102, 35 U.S.C. § 103, or 35 U.S.C. § 112.

D. Request for Withdrawal of Final Rejection of Claims 18, 20, and 21

In view of the fact that no specific statutory grounds for the rejection of claims 18, 20, or 21 have been recited in the Office Action mailed April 23, 2004, Applicants believe that the Finality of the Office Action should be withdrawn and, if a Notice of Allowance is not issued, a Supplemental Office Action should be issued reciting the statutory grounds for the Rejection of claims 18, 20, and 21.

Should the claims not be allowed, and the Finality of the Rejection not be withdrawn, the Board of Appeals presumably will require that the statutory grounds for rejection of claims 18, 20, and 21 be recited, if Applicants choose to appeal the Final Rejection.

E. **Discussion**

Stirton et al. U.S. Patent 6,614,540, one of the two references cited against all of Applicants' claims, was filed on June 28, 2001. In the accompanying Affidavit under 37 C.F.R. 1.131, Applicants' attorney, John P. Taylor, alleges, and demonstrates, in Exhibit A attached thereto, a conception date prior to the file date of the Stirton patent reference. The inventors submitted their disclosure to the Intellectual Property Department of LSI Logic Corporation, their employer, prior to the June 28, 2001 filing date of the Stirton patent. Thereafter, but prior to the filing date of the Stirton et al. reference, the Intellectual Property Department of LSI Logic Corporation reviewed the disclosure.

The Intellectual Property Department of LSI Logic Corporation then authorized the undersigned attorney, John P. Taylor (the Declarant in the Affidavit), to prepare a patent application on the subject matter of the Disclosure and file the patent application in the United State Patent and Trademark Office.

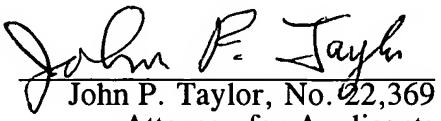
Applicants' attorney, after docketing and reviewing the disclosure, made a trip from Southern California to the offices of LSI Logic Corporation in Santa Clara, CA where he interviewed two of the three inventors (Colin Yates and Nicholas Eib). The third inventor, Nicholas Pasch, had, by this time, been terminated by LSI Logic Corporation. As stated in the Affidavit, Applicants' attorney then prepared a first draft of the patent application and sent it to the inventors (Colin Yates and Nicholas Eib) for their review. After some difficulty, Applicants' attorney was able to locate and contact the terminated inventor (Nicholas Pasch) at his home, and sent a copy of the first draft of the patent application to him there.

Applicants' attorney, after receiving the inventors' comments on the draft patent application, revised the patent application, prepared and had executed (by all of the inventors) the formal papers for the patent application, and then filed the patent application on November 30, 1991 by mailing the executed patent application to the USPTO by Express Mail on that date, as shown in exhibit D attached to the Declaration.

It should be noted that during the period of time extending from June 28, 2001, the filing date of the Stirton patent reference, and November 30, 2001, the filing date of applicants' patent application, two additional events occurred which further complicated the preparation and filing of Applicants' patent application (in addition to the fact that one of the inventors had been terminated by LSI Logic Corporation which made contact with this inventor more complicated). The September 11, 2001 bombing of the U.S. Trade Center buildings occurred during this period which resulted in disruption of communication, making it more difficult to communicate with, or travel to further interview, the inventors. Furthermore, LSI Logic announced within a few days of this national disaster, the permanent closing of the LSI Logic Corporation Santa Clara facility where the two remaining inventors had been employed (the announcement of the closing of the plant had actually been scheduled to be on September 12, 2001, but the events of September 11, 2001, and the resultant grieving of the nation dictated postponement of the announcement for a few days to a more opportune time).

In view of the foregoing remarks and the accompanying Declaration, it is believed that Applicants have established that their invention was conceived prior to the filing of the Stirton reference, and then constructively reduced to practice promptly thereafter so that the Stirton patent should be withdrawn as a reference. All of Applicants' now pending claims should then be patentable over the art. If the Examiner in charge of this case feels that there are any remaining unresolved issues in this case, the Examiner is urged to call the undersigned attorney at the below listed telephone number which is in the Pacific Coast Time Zone.

Respectfully Submitted,



John P. Taylor, No. 22,369
Attorney for Applicants
Telephone No. (909) 303-1416

Mailing Address:

Sandeep Jaggi, Chief Intellectual Property Counsel
LSI Logic Corporation
Legal Department- IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035

DOCKET NO. 01-234

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Colin D. Yates, Nicholas F. Pasch, and Nicholas K. Eib
Appl. No.	:	10/006,398
Filed:	:	November 30, 2001
Title	:	ALIGNMENT PROCESS FOR INTEGRATED CIRCUIT STRUCTURES ON SEMICONDUCTOR SUBSTRATE USING SCATTEROMETRY MEASUREMENTS OF LATENT IMAGES IN SPACED APART TEST FIELDS ON SUBSTRATE
Grp./ A.U.	:	2877
Examiner	:	Layla G. Lauchman
Docket No.	:	01-234

RULE 131 AFFIDAVIT OF JOHN P. TAYLOR, PATENT ATTORNEY FOR THE ASSIGNEE, LSI LOGIC CORPORATION

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

I, John P. Taylor, (Declarant) declares as follows:

1) That the Declarant is an attorney at law, registered to practice as a patent attorney by the United States Patent and Trademark Office;

2) That the Declarant has been engaged to represent LSI Logic Corporation before the United States Patent and Trademark Office for over ten years in a number of cases;

3) That Declarant represents LSI Logic Corporation before the USPTO in the present case, U. S. Patent Appl. Serial No. 10/006,398, wherein the claims have been rejected on a combination of references including Stirton U.S. Patent 6,614,540 (filed June 28, 2001);

4) That on a date prior to June 28, 2001, the filing date of the Stirton patent, an eight page disclosure (Exhibit A), describing the invention claimed in this case, was prepared by the three inventors, Colin D. Yates, Nicholas F. Pasch, and Nicholas K. Eib, which included, on page eight, the dated signatures of all three of the inventors, and the dated signatures of two witnesses, indicating that the two witnesses read and understood the Invention Disclosure;

5) That on a date prior to June 28, 2001, the filing date of the Stirton patent, the eight page disclosure was submitted by the named inventors to the Intellectual Property Department of the LSI Logic Corporation;

6) That after receiving and reviewing the patent disclosure prior to June 28, 2001, the filing date of the Stirton patent, the Intellectual Property Department of LSI Logic Corporation subsequently authorized the Declarant to prepare a patent application for filing in the USPTO (Exhibit B);

7) That the Declarant, upon receipt of the Authorization to prepare a patent application,(Exhibit B), and the inventors' Disclosure (Exhibit A), reviewed the disclosure, interviewed the inventors in a meeting with them at the offices of their employer, LSI Logic in Santa Clara, CA, prepared a draft of a patent application (Exhibit C) for review by the inventors, revised the patent application after receiving from the inventors their comments on the draft patent application, prepared and had executed the formal papers for the patent application, and then filed the patent application on November 30, 1991 by mailing the executed patent application to the USPTO by Express Mail on that date (Exhibit D);

8) The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made upon information and to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

06/09/04
Date

John P. Taylor
John P. Taylor

LSI LOGIC

Invention Disclosure Form

EXHIBIT A

LSI LOGIC CORP.
INTELLECTUAL PROPERTY DEPT.

Docket Number: 01-234

COPY

I. Title of Your Invention: ON THE USE OF LATENT RESIST IMAGE SCATTEROMETRY TARGETS TO IMPROVE THE ALIGNMENT CAPABILITY OF PHOTOLITHOGRAPHIC EXPOSURE TOOLS	Number of Attached Pages: RECEIVED [redacted] via E mail

Was your Invention first presented in an LSI Logic "Brainstorming Session?" (Y) (N) (unknown) (circle one)

If yes, specify the docket number assigned to you in the reminder e-mail:

II. List of All Inventors: (attach a separate sheet for additional inventors)

First Name*: Colin	M.I. *:D	Last Name*:Yates	
Home Address*:5977 Arabian Court, San Jose, CA 95123		Mail Stop*:J-202	Work Phone (408) 433 6484
LSI Employee*? (Y) (N) (unknown)	Vice President*:Richard Schinella	Citizenship*: British	Work Fax*:
If no, identify Employer*:	Manager*:Christopher Neville	Hire Date: Oct 1989	E-mail*:cyates @lsil.com
Job Title: Process Development Engineer	Department:		Home Phone: (408) 281 2315
First Name*: Nicholas	M.I. *:F	Last Name*: Pasch	
Home Address*: 1470 DESOLO DR PACIFICA, CA 94044		Mail Stop*:	Work Phone*:
LSI Employee*? (Y) (N) (unknown)	Vice President*:Richard Schinella	Citizenship*:USA	Work Fax*:
If no, identify Employer*:	Manager*:	Hire Date:	E-mail*:
Job Title:	Department:		Home Phone:
First Name*: Nicholas	M.I. *:K	Last Name*:Eib	
Home Address*: 781 Almondwood Way, San Jose, CA 95120		Mail Stop*:J-202	Work Phone*:
LSI Employee*? (Y) (N) (unknown)	Vice President*:Richard Schinella	Citizenship*:USA	Work Fax*:
If no, identify Employer*:	Manager*:	Hire Date:	E-mail*:eibn@lsil.com
Job Title:	Department:		Home Phone:
First Name*:	M.I. *:	Last Name*:	
Home Address*:		Mail Stop*:	Work Phone*:
LSI Employee*? (Y) (N) (unknown)	Vice President*:	Citizenship*:	Work Fax*:
If no, identify Employer*:	Manager*:	Hire Date:	E-mail*:
Job Title:	Department:		Home Phone:

III. Public Disclosure of Your Invention:

1. Was your Invention ever disclosed, either orally or in writing to anyone other than an LSI Logic employee*?
   (Y) (N) (unknown)
2. If yes to 1, specify the date(s) of disclosure*:
3. Are there plans to disclose your Invention in the future*? (Y) (N) (unknown)
4. If yes to 3, specify the date(s) of expected disclosure*:

IV. Use of Your Invention:

1. Has your Invention been used*? (Y) (N) (unknown)
2. If yes to 1, specify the date(s) of use*:
3. Are there plans to use your Invention in the future*? (Y) (N) (unknown)
4. If yes to 3, specify the date(s) of expected use*:

V. Invention "offered for" or "on sale":

1. Was a product or process containing your Invention "offered for sale" or "sold*?" (Y) (N) (unknown)
2. If yes to 1, specify the date(s) of the offer or sale*:

VI. Prior Art: (attach separate sheets if necessary) List only those patents, products, processes, journal articles, presentations, conferences, seminars, and other knowledge that you are aware of*, that are related to the subject matter of your Invention: (you have no duty to conduct a search)

Author/Event/Product/Process:	Title:	Date:
J.Bischoff, et al. 2001 SPIE Conference (Society of Photo-Optical Instrumentation Engineers). Metrology, Inspection, and Process Control for Microlithography.	Light diffraction based overlay measurement (Paper 4344-28)	Feb 2001
Ziad R. Hatab, et al. 1997 Proceedings of SPIE Conference (Society of Photo-Optical Instrumentation Engineers). Metrology, Inspection, and Process Control for Microlithography.	Optical diffraction tomography for latent image metrology (SPIE Vol. 3050 / 515).	1997
1.		
2.		

VII. Background to Your Invention: (attach separate sheets with your responses)

Describe:

1. The field to which your Invention pertains.

Semiconductor device manufacturing, and related fields using photolithography.

2. Problem(s) in the field which motivated your need to invent.

Accurately aligning one layer to an earlier layer.

3. Current approaches toward solving those problems (if any).

Exposure, development and measurement of a test wafer. Overlay errors measured on the test wafer can be corrected on subsequent wafers from the same lot.

4. Why those current approaches are unacceptable.

The assumption is made that the other wafers in the lot will behave the same as the test wafer. Any errors on the test wafer can only be corrected by reworking the wafer. It takes extra time to process and measure the test wafer while the rest of the lot is waiting.

VIII. Detailed Description of Your Invention: (attach separate sheets with your responses)

VIII. Detailed Description f Y ur Invention: (attach separate sheets with your resp nses)

1. Provide enough information and detail so that another person in your field could make and use your Invention*.

- If available, supplement your description with any existing reports, presentations, e-mails, sketches, drawings, schematics, photos, etc.
- At least one simple Figure or Flowchart of your Invention MUST be included*.

Scatterometry targets are patterned and etched into the previous layer to which alignment will occur. A typical example of a scatterometry target is a 100 x 100 um square of parallel straight lines.

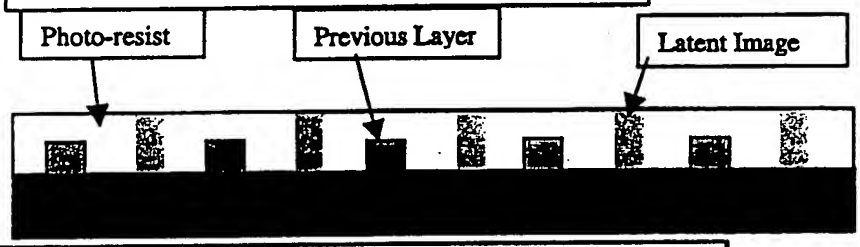
At the subsequent layer, the wafer is coated with photo-resist and loaded into the exposure tool. The alignment system of the tool is used to align the wafer, using any target appropriate to that tool.

The exposure tool then exposes a small number of test fields on the wafer. These can either be full fields, or small sub-sections of fields. The pattern that is exposed includes Scatterometry patterns that are exposed over the previous Scatterometry patterns. Th exposure will cause a latent image to be formed in the resist of the pattern that will subsequently be developed.

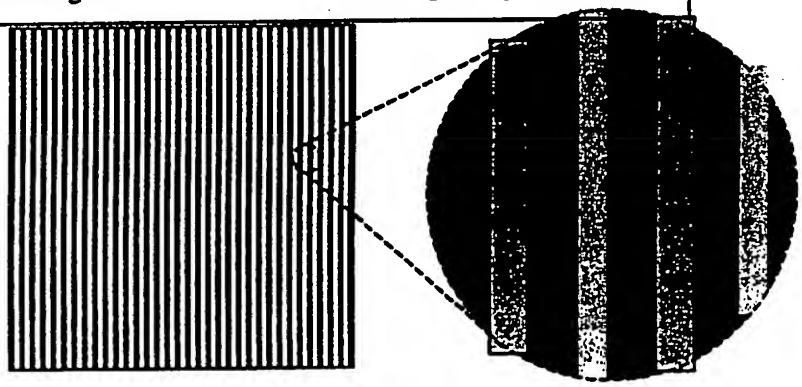
The combined Scatterometry target (the previous etched layer and the current layer latent image) is measured using a Scatterometry tool while the wafer is still on the exposure tool stage. The Scatterometry tool measures the overlay error between the current layer (latent resist image) and the previous layer.

The measurements of the Scatterometry target overlay errors are used to calculate alignment corrections for the wafer. The remaining fields on the wafer are exposed using these corrections.

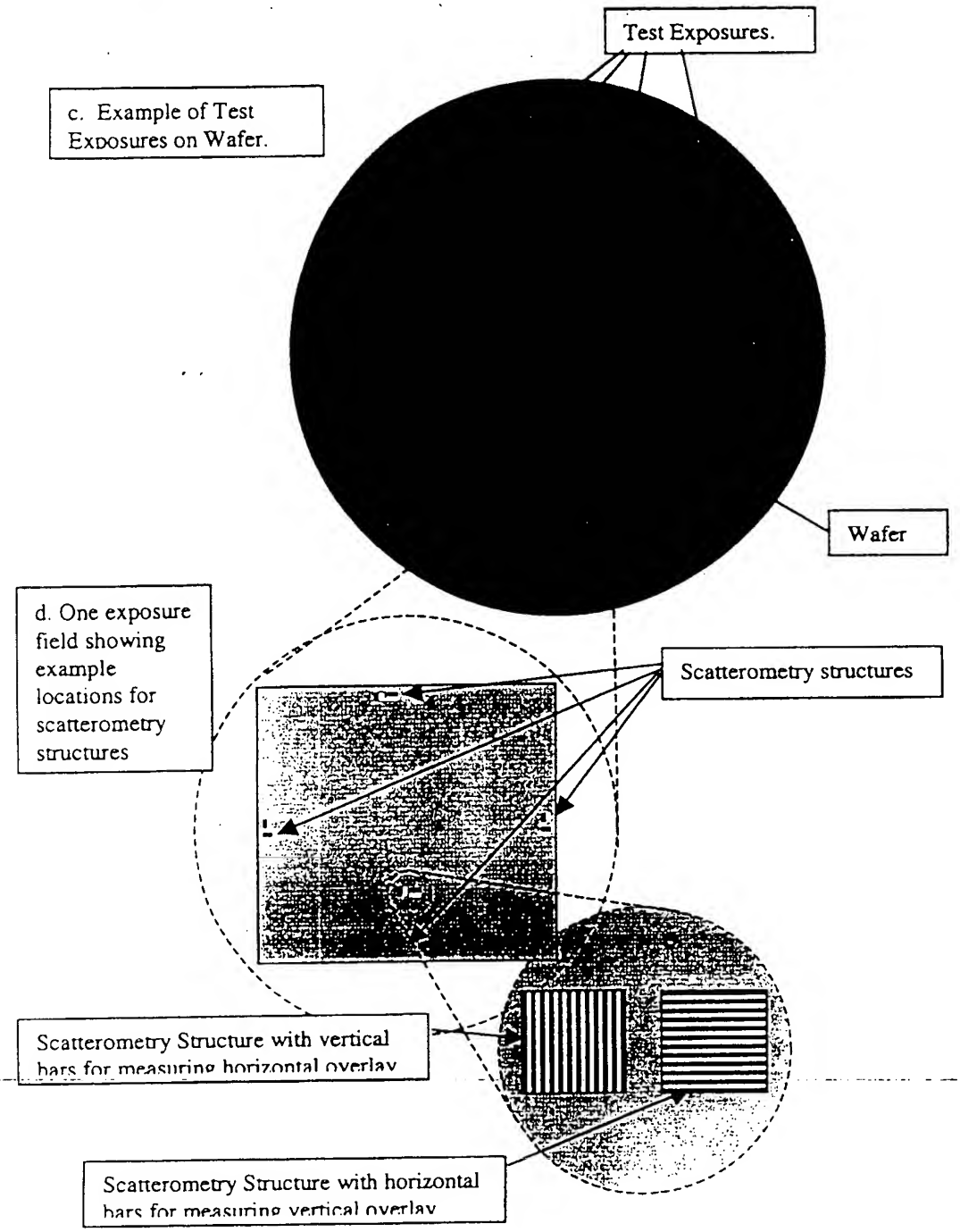
a. Cross Section of Scatterometry Structure made from alternating latent resist image and previous layer pattern



b. Top-down view of a Scatterometry Structure made from alternating vertical lines of latent resist image and previous layer



VIII. Detailed Description of Your Invention: (attach separate sheets with y ur responses)



2. Identify the new features of your Invention*.

Correction to the alignment of a wafer based on exposure of a small number of test fields on that same wafer, which are measured while the wafer is still in the tool, without any development of the resist image.

VIII. Detailed Description of Your Invention: (attach separate sheets with your responses)

3. List the advantages of your Invention*.

Corrections can be made individually to each wafer. There is no time required to develop a test wafer and measure the pattern overlay using an external tool.

4. Disclose alternate ways of making and using of your Invention.

a. This invention is based on the ability of Scatterometry tools to measure: 1. Latent image in resist. 2. Relative overlay of two layers in a process. This methodology can be applied to any other measurement tool that can perform both of these functions.

b. The measurement does not have to be made on every wafer in a lot. For example, the in-situ measurement could be made on the first wafer, and the resulting corrections then could be made to that wafer and the remaining wafers.

IX. Date of Your Invention:

1. Specify the date when you first conceived of your Invention*: (e.g. the conception date) [redacted]

2. Specify the date the first prototype was built*: (e.g. reduction to practice) NA

X. Customer/Vendor Contracts:

1. Was your Invention developed during performance of a customer/vendor contract*? (Y) (N) (unknown)

XI. Government March-In Rights:

1. Was your Invention conceived during performance of government contract*? (Y) (N) (unknown)

LSI LOGIC

Invention Disclosure Form

Docket Number: _____

BEST AVAILABLE COPY

XII. Signatures*: (sign only in BLUE ink)

We the aforementioned inventors submit in confidence this Invention disclosure to Attorneys within the LSI Logic Legal Dept. for the purpose of obtaining a legal opinion and/or legal advice as to the availability of patent, trade secret, and/or copyright protection for, and/or a general legal opinion or legal advice relating to the material contained within.

I(We) believe myself(ourselves) to be the first and original inventor(s) of this Invention:

	Inventor	Date:
1.	Colin [illegible],	[redacted]
2.	Nicholas F. Pasch	
3.	[illegible]	
4.		
5.		
6.		
7.		
8.		
9.		
10.		

Tw Witnesses who have read and understood this Invention disclosure*:

	Full Name of Witness (Print and Sign Name)	Date:
1.	Sarah Neumann [signature]	[redacted]
2.	Phong Do [signature]	[redacted]

The information within in this form has been provided to the LSI Logic Legal Department attorneys for the purpose of obtaining either a legal opinion, legal services, and/or assistance in a legal proceeding, and hence is privileged as an attorney-client communication.

EXHIBIT B

LSI Logic Int llectual Property Law Department Memo
Date: Tu sday, [redacted]
LSI Dock t Numb r: 01-234

Title : On The Use Of Latent R sist Image Scatterom try Targets To Improv The
Alignment Capability Of Photolithographic Expo ure Tools
Subject: Patent 01-234 - - LSI Authorization for Docket -01-234 - - Task - Preparation and
filing of original U.S. patent application in USPTO - Billing Code 4P-USP - Maximum amount
[redacted]

This is an authorization. The amount authorized for this task is the maximum amount to
be spent on completing the task. Upon completion of the task, please bill us for the
lesser of (1) the actual time spent on the task and (2) the maximum amount authorized.
We expect to be billed for the actual time spent on the task. Please do NOT bill us for the
maximum amount authorized unless the actual time spent equals or exceeds the

Key contributor(s)
1. Colin Yates, Ph: [+1] 408-433-6484, MS: AJ202, Email: cyates@lsil.com, Addr. : 5977 Arabian Ct, San Jose, CA 95123, VP: Richard
Schinella
2. Nicholas Pasch, Ph: Left LSI, MS: AJ201, Email: , Addr. : 1470 DESOLO DR, PACIFICA, CA 94044, VP: Richard Schinella
3. Nicholas Elb, Ph: [+1] 408-433-6465, MS: AJ202, Email: elbn@lsil.com, Addr. : 781 ALMONDWOOD WAY, SAN JOSE, CA 95120,
VP: Richard Schinella
Outside Counsel : John P. Taylor, TAYLOR, JOHN, Ph: (909) 699-7551, Email: DOTTEM@aol.com
LSI Attorney : Sandeep Jaggi, Ph: [+1] 408-954-4923, Email: jaggi@lsil.com
LSI Paralegal : Maria Kovacs, Ph: [+1] 408-433-8708, Email: mkovacs@lsil.com
LSI Liaison : Paul Rissman, Ph: [+1] 408-433-6380, Email: prissman@lsil.com
LSI Vice President : Richard Schinella, Ph: [+1] 408-433-6357, Email: richs@lsil.com
Technology Classification : PROCESS

1. Alignment: Mask/wafer
1. Photolithography (general)
1. Scatterometery

[redacted]
- Disclosure - Received from Inventor(s) - Thank you. Rec'd original ink-signed/witnessed disclosure....
- New Patent file opened
- Disclosure - Sent to Reviewer
- Disclosure - Received from Attorney with 1st review
- Disclosure - Received from Reviewer - Approved - REVIEW MEMO ANSWERS:
- Log - Sent reminder to Inventor(s) - Hi Colin and Nick: Per a recent change in procedure, all in...
- Disclosure - Sent to Attorney for final review - File w/review memo had been in Gary's office til now....
- Authorized preparation of 'first filed' application
- Award - Disclosure
- Disclosure - Received from Attorney with final review - file...
- Log - Emailed documents - TO : - Outside Counsel - DOTTEM@aol.com - Custom - DOTTEM@a...
- Due Date - to receive first draft

[redacted]

EXHIBIT C

JOHN P. TAYLOR
PATENT ATTORNEY
POST OFFICE BOX 1598
TEMECULA, CA 92593-1598
(909) 699-7551
(909) 699-7852 (Fax)

[redacted]

Dr. Colin D. Yates, M.S. J202
Dr. Nicholas K. Eib, M.S. J-202
LSI Logic Corporation
1551 McCarthy Blvd.
Milpitas, CA 95035

Re: Review of First Draft of Patent Application
Colin D. Yates, Nicholas F. Pasch, Nicholas K. Eib
ALIGNMENT PROCESS FOR INTEGRATED CIRCUIT STRUCTURES ON SEMICONDUCTOR SUBSTRATE USING SCATTEROMETRY MEASUREMENTS OF LATENT IMAGES IN SPACED APART TEST FIELDS ON SUBSTRATE
LSI Logic Docket No. 01-234

Dear Colin and Nicholas:

Enclosed for review and comment is a first draft of a patent application which has been prepared from your disclosure and the additional information which was discussed during our recent meeting at LSI Logic Corporation. You will note that this draft contains a number of questions which need to be addressed, as well as some blanks for the insertion of further information. Please review the application for accuracy and completeness, and let me have your comments. Please address each of the questions and blanks. Please also review the personal data, including correct spelling of names, middle initial, citizenship, and correct address.

Regards,

John P. Taylor

John P. Taylor
Patent Attorney

cc Sandeep Jaggi, Chief Intellectual Property Counsel, w/enclosure

DOCKET NO. 01-234
DRAFT NO. 1

EXPRESS MAILING LABEL NO. _____US

UNITED STATES PATENT APPLICATION FOR:

ALIGNMENT PROCESS FOR INTEGRATED CIRCUIT STRUCTURES ON SEMICONDUCTOR SUBSTRATE USING SCATTEROMETRY MEASUREMENTS OF LATENT IMAGES IN SPACED APART TEST FIELDS ON SUBSTRATE

By: **Colin D. Yates**
5977 Arabian Court
San Jose, CA 95123

Citizenship: United Kingdom

Nicholas F. Pasch
1470 Desolo Drive
Pacifica, CA 94044
DeSolo

Citizenship: U.S.A.

Nicholas K. Eib
781 Almondwood Way
San Jose, CA 95120

Citizenship: U.S.A.

ALIGNMENT PROCESS FOR INTEGRATED CIRCUIT STRUCTURES ON SEMICONDUCTOR SUBSTRATE USING SCATTEROMETRY MEASUREMENTS OF LATENT IMAGES IN SPACED APART TEST FIELDS ON SUBSTRATE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a process for alignment of vertically adjoining layers of an integrated circuit structure. More particularly this invention relates to an alignment process using scatterometry measurements of latent images in an upper layer of photoresist and a previously formed structural pattern in a lower layer in test fields on a semiconductor substrate.

2. Description of the Related Art

In the continuing reduction of scale in integrated circuit structures, both the horizontal dimensions of features such as metal lines and the spacing between such features have become smaller and smaller. This, in turn, has lead to an increased need for monitoring of the alignment of the features being formed on one layer of the integrated circuit structure with features already formed in an adjacent underlying layer.

Features such as metal lines, vias, trenches, etc. are usually formed on the integrated circuit structure by photolithography wherein a layer of photosensitive material is formed on the integrated circuit structure and selectively exposed to a pattern of radiation such as visible light through a mask or reticle. The radiation results in a chemical change in the portion of the photoresist exposed to the radiation, thereby forming a latent image of the patterned radiation in the photoresist layer corresponding to a change in solubility between the exposed and unexposed portions of the photoresist layer. The latent image is then developed by baking the photoresist layer followed by contact of the baked and exposed photoresist layer with an etchant or developer resulting in removal of either the exposed or unexposed portion of the photoresist layer, depending upon the type of etchant or developer selected, thereby forming a photoresist mask which can be used to form features such as metal lines.

Accuracy of the formation of features in a particular layer of an integrated circuit structure has been optically monitored using scanning electron microscopy (SEM) on a test wafer, followed by adjustments made to correct errors before proceeding with the run of wafers in which the same pattern of features would be reproduced. More recently scatterometry techniques have been used to monitor defects in a test wafer, wherein radiation is reflected or scattered off targeted features arranged in a diffraction pattern on a test wafer and the degree of alteration or scattering of the diffracted light is detected and compared to known patterns of alteration or scattering of the diffracted light, following which suitable adjustments are made before proceeding with the run of wafers, as in the previous SEM monitoring. In either instance, however, an entire test wafer is expended to accomplish the desired testing of the accuracy of the features. Furthermore, although scatterometry has been used to measure latent (undeveloped) images in a single photoresist layer, conventionally, the latent image is developed (by baking of the resist layer and then contacting it with a wet developer or etchant) prior to optical measurement of the resist mask.

Accurate alignment of the features in a particular layer of the integrated circuit structure with features in an underlying layer is also important and must also be monitored. Such monitoring has also been carried out using SEM technology as well as scatterometry. A pattern of parallel lines in one layer, typically a pattern of parallel lines in a 100 nm by 100 nm square, is either aligned directly over an identical pattern of lines in the preceding layer, or the two layers of parallel lines are arranged as alternate lines, i.e., the parallel lines in the first layer are arranged such that the parallel lines in the second layer are seen in the spaces between the parallel lines in the first layer and the accuracy of the spacing of the pattern of lines in the upper level to the underlying pattern of lines is measured. However, this has required the use of a test wafer wherein the latent images on the exposed photoresist mask layer are first baked and developed and then analyzed for alignment with the alignment pattern in the underlying layer, necessitating the use of the entire wafer.

It would, therefore, be desirable if the alignment of features on vertically adjoining layers in an integrated circuit structure could be optically monitored without the expenditure of an entire test wafer, and without requiring the development of latent images already formed in selected fields of an upper layer on the wafer.

SUMMARY OF THE INVENTION

The invention comprises a process for measuring alignment of latent images in selected fields of a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in the same selected fields of a lower layer on the substrate by the steps of:

a) forming a test pattern in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over the first layer;

c) forming latent images in portions of the photoresist layer lying in the selected fields overlying the test pattern of the first layer; and

d) measuring the alignment of the test pattern in the selected fields of the first layer with the overlying latent images in the photoresist layer using scatterometry.

In a preferred embodiment, the test pattern formed in each of the selected fields in the first layer comprises a pattern of parallel spaced apart lines, and the latent images formed in the portions of the photoresist layer in the selected fields above the test pattern in the first layer also comprises a pattern of parallel spaced part lines, with the two sets of lines interspaced between one another and generally parallel to one another to form a diffraction pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a fragmentary vertical side-section view of a portion of an integrated circuit structure having a test pattern of parallel spaced apart metal lines formed thereon.

Figure 2 is a fragmentary vertical side-section view of the structure of Figure 1 showing a layer of photoresist formed over the integrated circuit structure and over the test pattern of parallel spaced apart metal lines thereon.

Figure 3 is a fragmentary vertical side-section view of the structure of Figure 2 showing a pattern of latent images comprising parallel spaced apart lines being formed in the photoresist layer in between the parallel spaced apart metal lines by selective exposure of the photoresist layer to patterned radiation through a reticle or mask.

Figure 4 is a sectioned top view of the structure of Figure 3 taken along lines 4-4.

Figure 5 is a fragmentary vertical side-section view of the structure of Figure 3 showing a scatterometry radiation source being directed at an angle against the pattern of spaced apart parallel metal lines and lines of latent images in the photoresist layer, and the image of diffracted radiation being detected.

Figure 6 is a top view of a semiconductor wafer having preselected test fields A-D in which the test images of metal lines and latent images of lines are formed.

Figure 7 is a flowsheet illustrating the process of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention comprises a process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate by the steps of: forming a test pattern in selected fields of a first layer on a semiconductor substrate; forming a layer of photoresist over the first layer; forming latent images in portions of the photoresist layer lying in the selected fields overlying the test pattern of the first layer; and measuring the alignment of the test pattern in the selected fields of the first layer with the overlying latent images in the photoresist layer using scatterometry.

In a preferred embodiment, the test pattern formed in each of the selected fields in the first layer comprises a pattern of parallel spaced apart lines, and the latent images formed in the portions of the photoresist layer in the selected fields above the test pattern in the first layer also comprises a pattern of parallel spaced part lines, with the two sets of lines interspaced between one another and generally parallel to one another to form a diffraction pattern.

Referring now to the drawings, Figure 1 shows a fragmentary portion 2 of an integrated circuit structure on a semiconductor wafer (not shown) having a test pattern of parallel spaced apart metal lines 6 formed over integrated circuit structure 2. This test pattern of parallel metal

lines 6 is used for alignment with latent images of a second set of lines formed in an overlying photoresist layer as will be explained below. Integrated circuit structure 2 may comprise active devices such as transistors having an insulation layer formed thereon, with metal lines 6 then formed over the insulation layer.

The test pattern of parallel metal lines 6 is configured to occupy either all or a portion of one field on the semiconductor wafer, where a field is defined as that portion or position on a semiconductor wafer on which a single chip or integrated circuit structure will be formed. It may also be defined as that portion of a wafer individually addressed by a stepper tool to photolithographically process that portion of the wafer independent of the remainder of the wafer. The same or different structures or patterns may then be constructed in other fields representing different positions on the wafer which are sequentially addressed individually by the stepper tool. NOTE TO INVENTORS: IS THIS A SATISFACTORY DEFINITION OF THE TERM "FIELDS" AS USED HEREIN? IF NOT, PLEASE CORRECT OR ADD TO AS NEEDED. THIS IS IMPORTANT BECAUSE TERM WILL BE USED IN CLAIMS.

As will be noted in Figure 6, such test patterns of parallel spaced apart metal lines 6 are formed in at least a portion of several test fields distributed across the wafer, as indicated by arrows A-D in Figure 6, to provide more uniform measurement of the alignment across the entire wafer.

As shown in Figure 2, after formation of the test patterns in selected fields distributed across the wafer, a layer 10 of photoresist is formed over the entire wafer in a thickness sufficient to cover metal lines 6. Latent images 16 of a second set of parallel spaced apart lines are then formed in photoresist layer 10, using a mask or reticle 20 containing openings 24 through which a radiation image is directed for the same field that is occupied by underlying metal lines 6, as seen in Figure 3.

The term "latent images", as used herein is meant a pattern of radiation (but undeveloped) portions of a photosensitive material wherein such radiation exposure changes the solubility of such exposed portions to certain solvents (developers) relative to the unexposed regions of the photosensitive material. Conventionally such "latent images" are developed by contact

with a solvent or "developer" which dissolves either the exposed or unexposed portion of the photosensitive material to thereby form a photoresist mask.

In accordance with the invention, the undeveloped or "latent image" is used in the alignment process of the invention, not the developed image, to verify the alignment (or measure the degree of alignment) between the pattern of lines (latent images at this point) formed in the photoresist layer with the underlying pattern of parallel spaced apart metal lines. By using the undeveloped latent images for verification of alignment with the underlying metal lines, misalignment problems shown in the test fields can be corrected (e.g., by adjustment of the reticle mount) and the remaining fields of the wafer being tested may then be exposed to the actual pattern of integrated circuit structure (e.g., a pattern of metal interconnects instead of the pattern of test lines) and such images may then be developed for such fields. In this way, the entire wafer is not expended as a test wafer to verify the alignment of features such as lines on the respective layers.

The latent images formed in the photoresist layer may be used as a means of verification of the alignment by positioning the underlying metal lines, with respect to the reticle which will be used to form the overlying latent images of parallel lines, so that the overlying latent images of lines, when formed, will each be equally spaced between two adjacent metal lines, as shown in Figure 4, where line latent images 16 in photoresist layer 10 aré shown as equally spaced between metal lines 6 (the theoretical perfect alignment).

Such initial alignment between the pattern of metal lines and the reticle can be made by visual inspection and alignment of the reticle mount with a larger target on the first layer followed by precise verification of the alignment using the process of the invention. In accordance with the invention, the precise alignment of the underlying pattern of parallel spaced apart metal lines with the pattern of latent images in the photoresist layer is carried out using scatterometry apparatus.

J.R. Buell, in an article entitled "Scatterometry Applied to Microelectronics Processing", published in Volume 14, Number 5 of the IEEE Lasers and Electro-Optics Society Newsletter in October, 2000, at pages 26-27, defines scatterometry as a non-destructive optical technique

that records and analyzes changes in the intensity of light reflected from a periodic scattering surface. The author states that by measuring and analyzing the light diffracted from a patterned periodic sample, the dimensions of the sample itself can be measured, and says that scatterometry exploits the sensitivity of diffraction from a sample to changes in the line-shape of the sample. NOTE TO INVENTORS: ARE YOU SATISFIED WITH THIS EXPLANATION OF "SCATTEROMETRY"? IF NOT, PLEASE FURNISH A PUBLISHED ARTICLE WITH A BETTER DEFINITION. I AM QUOTING FROM A PUBLISHED ARTICLE TO AVOID HAVING THE PATENT EXAMINER REJECT US FOR FAILING TO DEFINE THE TERM AND ESTABLISH IT AS AN ART-RECOGNIZED TERM.

In the usage of such scatterometry technology in accordance with the invention, a radiation source 30, as shown in Figure 5, is directed at an angle onto the respective patterns of metal lines 6 and latent images 16 whereby the metal lines and latent images function together as a diffraction gradient to scatter the radiation. The scattered radiation is then detected by one or more detectors 34 and compared with known patterns of scattered radiation to determine the extent of the variation from a perfect spacing of the latent images 16 with metal lines 6. Such scatterometry tools are commercially available from the _____ Company under the trademark _____, and from the _____ Company under the trademark _____. NOTE TO INVENTORS: PURPOSE OF IDENTIFYING COMMERCIAL EQUIPMENT DESIGNED TO USE SCATTEROMETRY IS BOTH FOR COMPLETENESS OF DESCRIPTION AS WELL AS TO AGAIN EMPHASIZE THAT SCATTEROMETRY IS RECOGNIZED IN THE ART.

It should be noted that the radiation source used in the scatterometry apparatus and diffracted by the latent images formed in the photoresist layer must be of a wavelength at which the photoresist layer is not sensitive, i.e., at a wavelength different than the wavelength used to form the latent image in the photoresist layer through the reticle, to avoid exposing the entire photoresist layer to radiation at the wavelength used to form the latent image, i.e., to avoid turning the entire photoresist layer into one latent image. This could be carried out, for example, by using photoresist material sensitive to UV light, but not sensitive to visible light, and then using visible light as the radiation source in the scatterometry apparatus. NOTE TO

INVENTORS: IF THE LATENT IMAGES ARE FORMED IN A PHOTORESIST MATERIAL SENSITIVE TO RADIATION REACHING THE PHOTORESIST MATERIAL THROUGH THE RETICLE, WHAT KEEPS THE RADIATION SOURCE IN THE SCATTEROMETRY APPARATUS FROM EXPOSING THE REMAINDER OF THE PHOTORESIST MATERIAL IN THE PARTICULAR FIELD? IS THERE SOME WAVELENGTH SENSITIVITY INVOLVED HERE WHEREIN THE PHOTORESIST MATERIAL IS NOT PHOTO-SENSITIVE TO THE RADIATION WAVELENGTH USED IN THE SCATTEROMETRY APPARATUS?

Following the alignment step, the data concerning any misalignment can be used to move the reticle, with respect to the underlying wafer having the layer of metal lines thereon, so that the remainder of the fields in the wafer can then have an aligned layer subsequently formed thereon.

By only using selected fields of the semiconductor wafer distributed across the face of the wafer to form the test patterns of lines, as shown at arrows A-D in Figure 6, and then not developing the latent images formed in those fields in order to align the two layers to one another, and by exploiting the ability of scatterometry technology to detect latent images, only selected fields of a wafer need be used to align an underlying pattern of parallel spaced apart metal lines with a pattern of latent images of lines in an overlying photoresist layer.

With the alignment process of the invention, rather than expending an entire test wafer and then relying on the alignment adjustments made on such a wafer to suffice for the remaining wafers in the same batch, each wafer amy be subject to the alignment process of the invention to detect and then correct any misalignment detected in the test fields by the scatterometry apparatus, following which the other fields in the same wafer (which should now be precisely aligned) may be used to form the desired layer over the underlying integrated circuit structure.

It should be noted that the process of the invention makes it possible to utilize two sets of test fields on a particular wafer, if desired. That is, a first set of test fields may be used, as described, to verify the alignment of the reticle with the underlying layer using the latent images formed by the reticle in the photoresist layer, followed by adjustment of the reticle.

A second set of latent images of lines could then be formed in a second set of test fields to verify that the corrections already made are satisfactory. Since this would expend, for example, 8 fields instead of only 4, it may be more desirous to only use one set of test fields. However, in view of the fact that wafers such as the _____" diameter wafers currently in production, have as many as _____ fields, the expenditure of either 4 or 8 fields may be deemed to be a small price to pay for verification of the accuracy of the alignment.

Thus, the invention utilizes scatterometry technology to analyze the alignment of a pattern of latent images (such as parallel lines) formed in an upper photoresist layer with an underlying pattern (such as parallel lines) formed in selected test fields on a semiconductor wafer. The remaining fields on the same wafer may then be utilized to form the desired integrated circuit structures on the wafer tested. The process of the invention avoids the need for expenditure of an entire test wafer to verify the alignment and also permits each individual wafer to be tested for alignment, and corrected where needed.

Having thus described the invention what is claimed is:

1. A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images in portions of said photoresist layer lying in said selected fields overlying said test pattern of said first layer; and

d) measuring the alignment of said test pattern in said selected fields of said first layer with said overlying latent images in said photoresist layer using scatterometry.

2. The process of claim 1 wherein said test pattern formed in said selected fields of said first layer comprises a test pattern of lines.

3. The process of claim 2 wherein said test pattern of lines formed in said selected fields of said first layer comprises a test pattern of parallel spaced apart lines.

4. The process of claim 2 wherein said test pattern of lines formed in said selected fields of said first layer comprises a test pattern of parallel spaced apart metal lines.

5. The process of claim 3 wherein said latent images formed in said portions of said photoresist layer lying in said selected fields overlying said test pattern of lines comprises a pattern of parallel spaced apart lines.

6. The process of claim 5 wherein said latent images of parallel spaced apart lines, formed in said portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel spaced apart lines formed in said selected fields of said first layer, are formed generally parallel to said test pattern of parallel spaced apart lines formed in said selected fields of said first layer, whereby said test pattern of parallel spaced apart lines formed in said selected fields of said first layer and said latent images of parallel spaced apart lines formed in said portions of said photoresist layer lying in said selected fields form a diffraction grating, the accuracy of which is measured by said scatterometry to determine the alignment of said layers of lines.

7. The process of claim 6 wherein said latent images of parallel spaced apart lines are interspaced between said test pattern of parallel spaced apart lines formed in said selected fields of said first layer.

8. A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern of parallel spaced apart lines in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images of parallel spaced apart lines in portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel lines of said first layer, said parallel lines of said test pattern of said first layer generally parallel with said parallel lines of latent images in said photoresist layer; and

d) measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry.

9. The process of claim 8 wherein said test pattern of parallel spaced apart lines formed in said selected fields of said first layer comprises a test pattern of parallel spaced apart metal lines.

10. The process of claim 8 wherein said latent images of parallel spaced apart lines formed in said photoresist layer and said test pattern of parallel spaced apart lines formed in said first layer are formed generally parallel to one another to form a diffraction grating, the accuracy of which is measured by said scatterometry to determine the alignment of said layers of lines.

11. The process of claim 10 wherein said latent images of parallel spaced apart lines are interspaced between said test pattern of parallel spaced apart lines formed in said first layer.

12. The process of claim 8 wherein said step of forming latent images of parallel spaced apart lines in said photoresist layer further comprises directing a first source of radiation onto said photoresist layer through a reticle patterned to provide a radiation image of said parallel spaced apart lines on said photoresist layer.

13. The process of claim 12 wherein said step of measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry further comprises directing a second source of radiation toward said latent images of lines in said photoresist layer and toward said test pattern of parallel spaced apart lines in said first layer, wherein said photoresist layer is photosensitive to said first source of radiation but not to said second source of radiation.

14. The process of claim 12 wherein said first source of radiation used to form said latent images in aid photoresist layer comprises ultraviolet light.

15. The process of claim 12 wherein said second source of radiation used in said scatterometry to determine said alignment comprises visible light.

16. The process of claim 8 including the further step of forming a layer of metal interconnects over said first layer on said integrated circuit structure in fields not used for said alignment.

17. A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate which comprises:

a) forming a test pattern of parallel spaced apart metal lines in selected fields of a first layer on a semiconductor substrate;

b) forming a layer of photoresist over said first layer;

c) forming latent images of parallel spaced apart lines in portions of said photoresist layer lying in said selected fields overlying said test pattern of parallel lines of said first layer, said parallel lines of said test pattern of said first layer generally parallel with said parallel lines of latent images in said photoresist layer;

d) measuring the alignment of said parallel lines of said test pattern in said selected fields of said first layer with said overlying latent images of parallel lines in said photoresist layer using scatterometry; and

e) forming a further layer of integrated circuit structure over said first layer on said integrated circuit structure in fields not used for said alignment.

18. The process of claim 17 wherein said step of forming a further layer of integrated circuit structure over said first layer further comprises forming a layer of metal interconnects over said first layer on said integrated circuit structure in fields not used for said alignment.

ABSTRACT OF THE INVENTION

A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate comprises the steps of forming a test pattern in selected fields of a first layer on a semiconductor substrate, forming a layer of photoresist over the first layer, forming latent images in portions of the photoresist layer lying in the selected fields overlying the test pattern of the first layer; and measuring the alignment of the test pattern in the selected fields of the first layer with the overlying latent images in the photoresist layer using scatterometry. In a preferred embodiment, the test pattern formed in each of the selected fields in the first layer comprises a pattern of parallel spaced apart lines, and the latent images formed in the portions of the photoresist layer in the selected fields above the test pattern in the first layer also comprises a pattern of parallel spaced part lines, with the two sets of lines interspaced between one another and generally parallel to one another to form a diffraction pattern.

01-234

Fig. 1

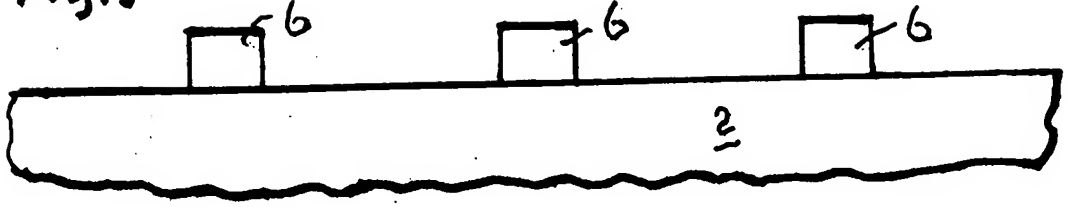


Fig. 2

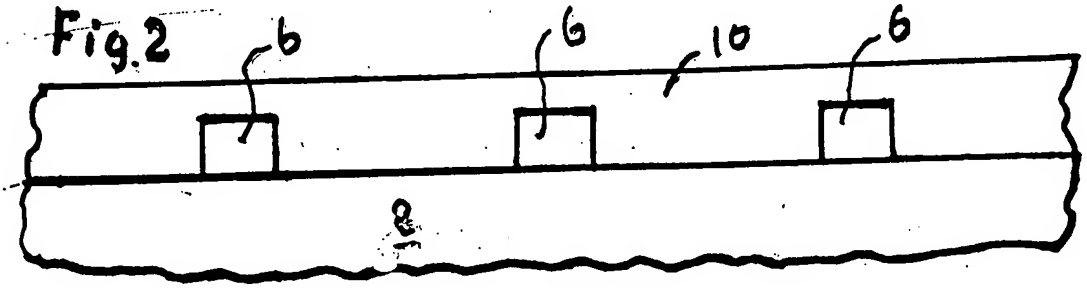


Fig. 3

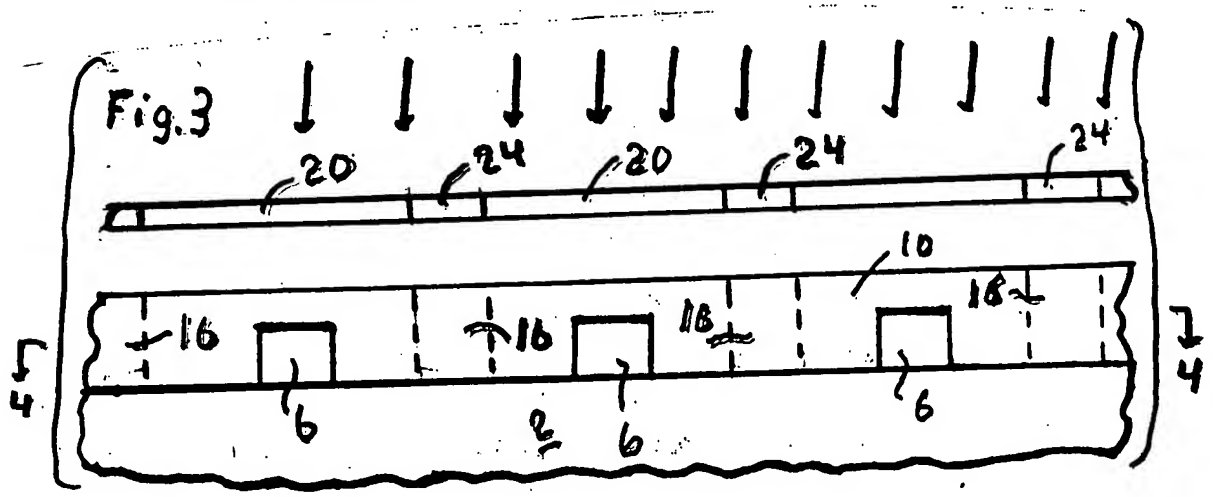
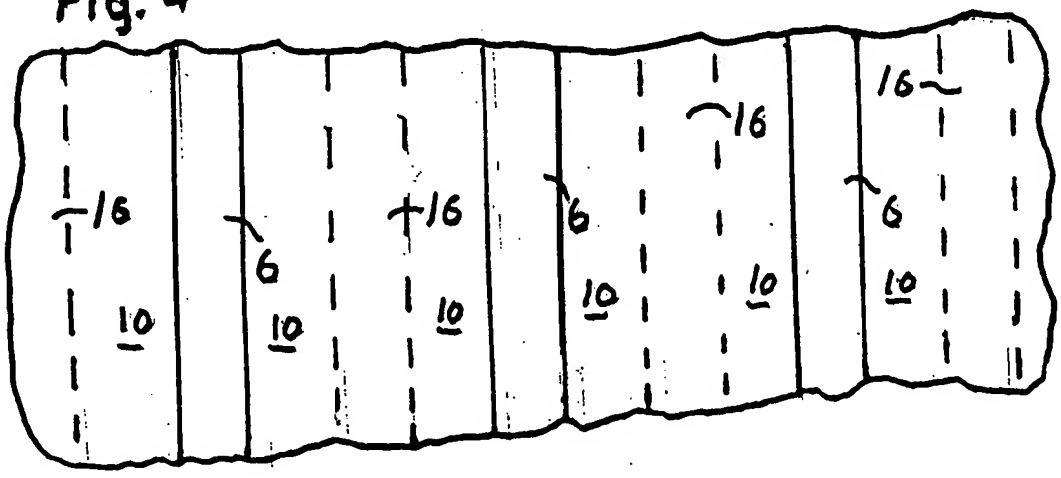


Fig. 4



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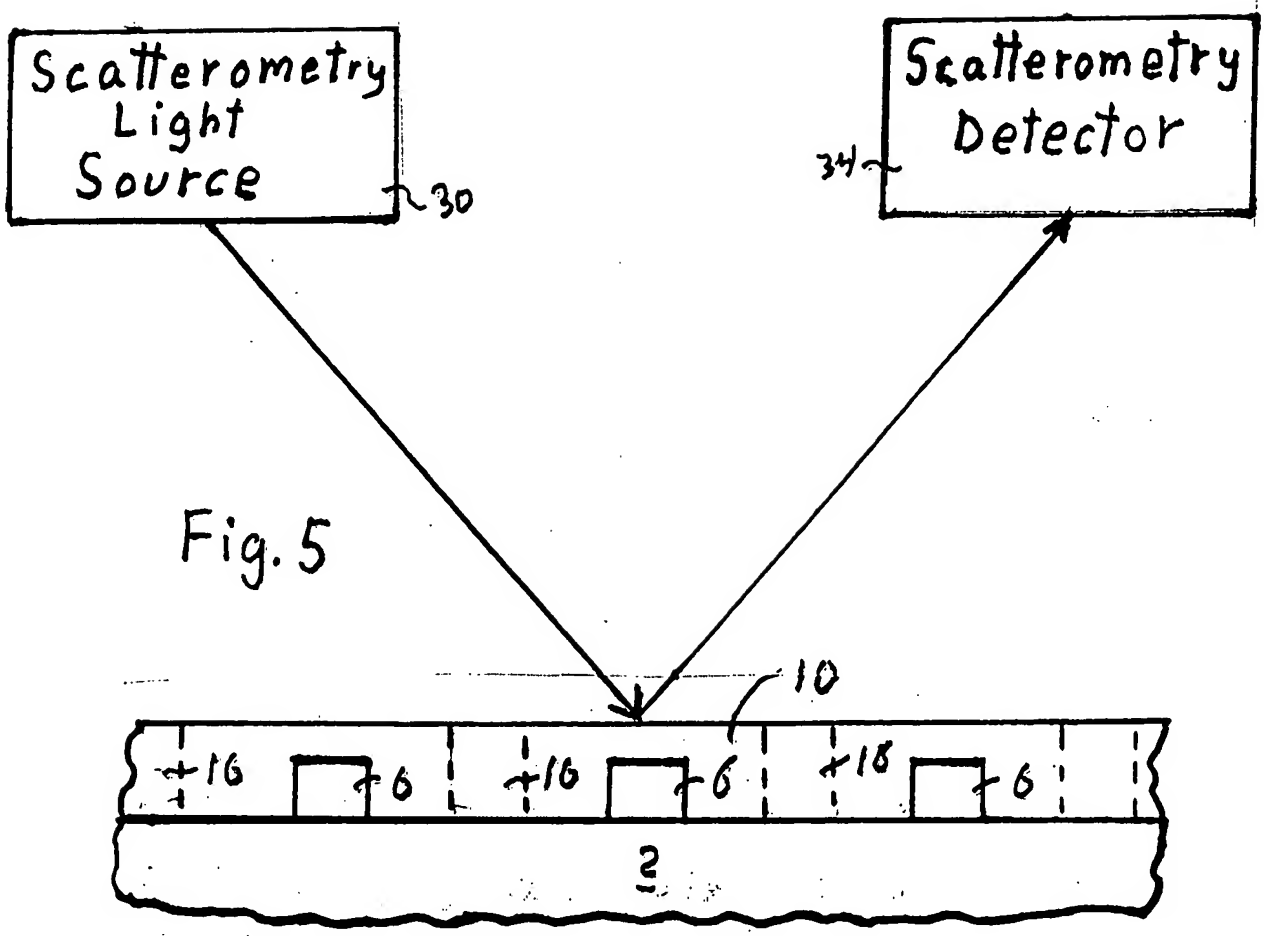

Fig. 5

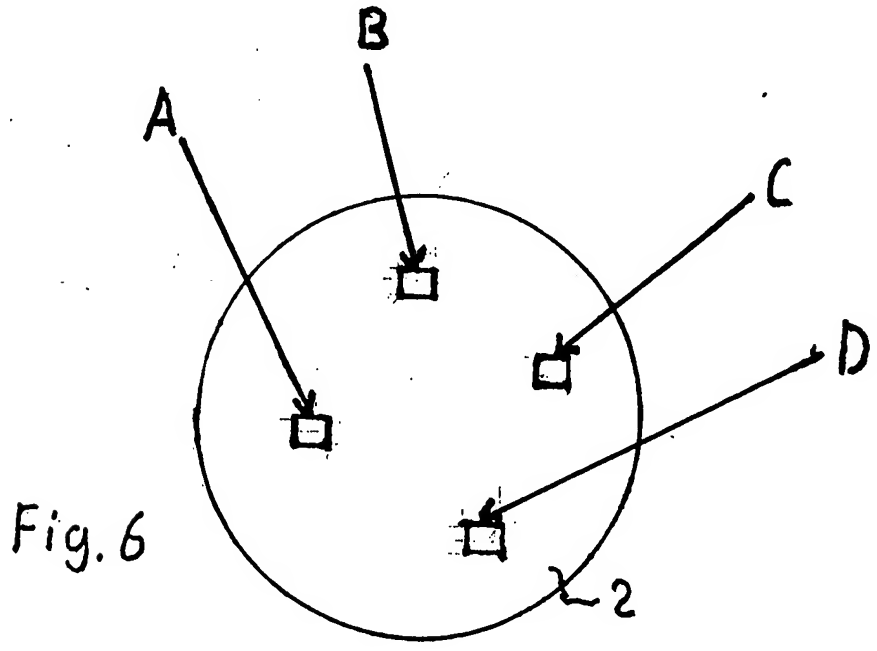

Fig. 6

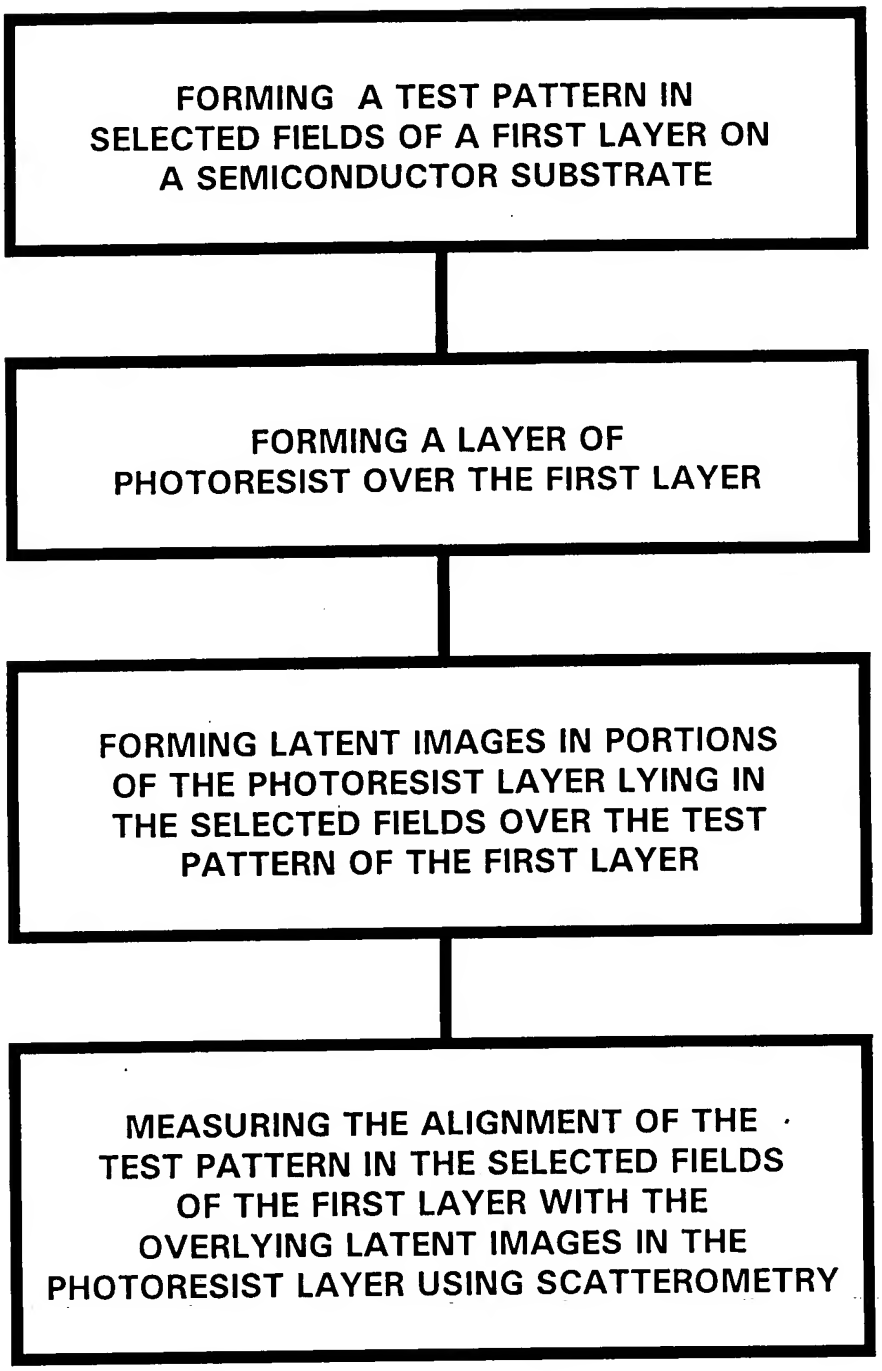
FORMING A TEST PATTERN IN SELECTED FIELDS OF A FIRST LAYER ON A SEMICONDUCTOR SUBSTRATE
FORMING A LAYER OF PHOTORESIST OVER THE FIRST LAYER
FORMING LATENT IMAGES IN PORTIONS OF THE PHOTORESIST LAYER LYING IN THE SELECTED FIELDS OVER THE TEST PATTERN OF THE FIRST LAYER
MEASURING THE ALIGNMENT OF THE TEST PATTERN IN THE SELECTED FIELDS OF THE FIRST LAYER WITH THE OVERLYING LATENT IMAGES IN THE PHOTORESIST LAYER USING SCATTEROMETRY

FIGURE 7

EXHIBIT D

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